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DATE: Tuesday, June 07, 2005 Printable Copy Create Case

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L5	rewritable or $dram or (random adj1 access adj1 memory) or ram	519656	L5
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L6: Entry 5 of 10 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6282310 B1

**** See image for Certificate of Correction ****

TITLE: Image processing apparatus, method, and image processing system

Detailed Description Text (10):

The data scrambling circuits 7 and 18 can be any circuit as long as they can set a reversible conversion function, and a LUT using a RAM is provided as an example. The advantage of a data scrambling circuit using a RAM is that the function can be easily changed. However, since the RAM is for a general-purpose, a data scrambling circuit 7 is easily composed, thus even if an image processing apparatus is not an authorized one, as far as it comprises the same data scrambling circuit 7, it can be connected to the image forming apparatus 2 of this embodiment to make the image forming apparatus 2 print an image. Therefore, in this embodiment, a data scrambling circuit 7 is constructed with a custom IC formed from a programmable gate array.

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☐ 1. Document ID: US 6282310 B1

L7: Entry 1 of 1 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6282310 B1
**** See image for Certificate of Correction ****
TITLE: Image processing apparatus, method, and image processing system

Brief Summary Text (13):
First, the image data is processed in the image processing circuit 6, then applied with a data conversion function f in a data scrambling circuit using a ROM, and is sent to the image forming apparatus 2. The image forming apparatus 2 applies an inverse data conversion function f.sup.-1 to the received image data, and then reproduces the image data. Thus, the data conversion function f is a reversible function, and the image data before conversion and after conversion is the same. The data conversion function f is written in the ROM in the data scrambling circuit of the image processing apparatus 1, and the inverse data conversion function f.sup.-1 is written in the ROM in the data scrambling circuit of the image forming apparatus 2, both as LUTs (look up tables).

Detailed Description Text (10):
The data scrambling circuits 7 and 18 can be any circuit as long as they can set a reversible conversion function, and a LUT using a RAM is provided as an example. The advantage of a data scrambling circuit using a RAM is that the function can be easily changed. However, since the RAM is for a general-purpose, a data scrambling circuit 7 is easily composed, thus even if an image processing apparatus is not an authorized one, as far as it comprises the same data scrambling circuit 7, it can be connected to the image forming apparatus 2 of this embodiment to make the image forming apparatus 2 print an image. Therefore, in this embodiment, a data scrambling circuit 7 is constructed with a custom IC formed from a programmable gate array.

Detailed Description Text (43):
The RGB image data (luminance information) read from the image memory 5 is converted to CMY image data (density information) in a logarithmic conversion LUT 61 on the basis of processing information stored in a control register 64. The CMY image data outputted from the logarithmic conversion LUT 61 is then converted to CMYK image data in a color space converter 62.

Detailed Description Text (46):
The density of the CMYK image data outputted from the color space converter 62 is corrected in a density correction unit 63 which is composed of a LUT for each color. The density correction is a process to apply corrections corresponding to density characteristics of the image forming apparatus 2 (.gamma. correction). Thus, the correction must correspond to the aforesaid condition of the image forming apparatus 2, and correction coefficients may frequently change compared to coefficients used in the color space conversion. The contents of the LUTs are

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L6: Entry 4 of 10 File: USPT May 14, 2002

DOCUMENT-IDENTIFIER: US 6389525 B1
TITLE: Pattern generator for a packet-based memory tester

Detailed Description Text (15):
To provide for conventional X and Y address scrambling, respective X and Y address scrambling circuits 146 and 148 are disposed between the pattern generator input and output multiplexer arrays 60 and 166. The scrambling circuits include respective 256K X and Y scramble RAMS 150 and 152 that act as lookup tables between the physical and logical X and Y addresses. The outputs of the scramble RAMs connect to respective selectors 154 and 156 that distribute the scrambled signals along respective X and Y scrambled address busses 158 and 160. Respective bypass connections 162 and 164 couple the unscrambled X and Y address signals to the selectors 154 and 156.

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